

Amendments to the Claims

1-7. (Cancelled)

8. (Currently Amended) A three-dimensional (3-D) integrated chip system, comprising:

a first wafer including one or more integrated circuit (IC) devices, a first plurality of metallic bonding pads deposited via an interlevel dielectric (ILD) for wafer-to-wafer bonding and electrical interconnection, the first plurality of metallic bonding pads having a variety of heights, and an ILD recess surrounding the first plurality of metallic bonding pads deposited via the ILD; and

a second wafer including one or more integrated circuit (IC) devices, a second plurality of metallic bonding pads deposited via an interlevel dielectric (ILD) for wafer-to-wafer bonding and electrical interconnection, the second plurality of metallic bonding pads having a variety of heights, and an ILD recess surrounding the second ~~first~~ plurality of metallic bonding pads deposited via the ILD,

wherein the first plurality of metallic bonding pads is bonded to the second plurality of metallic bonding pads to establish electrical connections between active IC devices on the adjacent wafers, and

wherein the ILD is a high-temperature deformable dielectric used to allow the bonding areas to be self-leveling to facilitate the bonding of wafers having bonding pads of a variety of heights,

wherein the high-temperature deformable dielectric is SILK which exhibits a glass transition near 450°C while the metallic bonding pads exhibit a bonding temperature of about 400°C, and

wherein the ILD recesses are created by a Chemical Mechanical Polish (CMP) or by selectively etching the ILD surrounding the metallic bonding pads deposited via the ILD.

9. (Currently Amended) The three-dimensional (3-D) integrated chip system as claimed in claim 8, wherein the metallic bonding pads include Copper (Cu) bonding pads deposited on opposing surface of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers.

10-13. (Cancelled)

14. (Currently Amended) A three-dimensional (3-D) integrated chip system, comprising:
a first wafer including one or more integrated circuit (IC) devices;
a second wafer including one or more integrated circuit (IC) devices; and
metallic lines deposited on opposing surfaces of the first and second wafers at designated locations with an interlevel dielectric (ILD) recess, created by a chemical mechanical polish or by selectively etching the ILD surrounding the metallic lines, surrounding the metallic lines to facilitate direct metal bonding between the first and second wafers and establish electrical connections between active IC devices on the first and second wafers, wherein the ILD is a high-temperature deformable dielectric used to allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers to be bonded, wherein the high-temperature deformable dielectric is SILK which exhibits a glass transition near 450°C while the metallic lines exhibit a bonding temperature of about 400°C.

15. (Previously presented) The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the metallic lines include a plurality of Copper (Cu) bonding pads on opposing surface of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers.

16-19. (Cancelled)

20. (Previously presented) The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the first wafer is thinner than the second wafer to conform to height differences of the metallic lines across opposing surfaces of the adjacent wafers.

21-26. (Cancelled)